CLAIMS

1. A method for manufacturing an integrated circuit, the method comprising:

(1) obtaining a structure comprising:

a semiconductor substrate having a plurality of first areas which are to include one or more active areas of one or more nonvolatile memory cells;

one or more dielectric regions for providing isolation between at least two of the first areas, each dielectric region having a portion below the top surface of the substrate, the dielectric regions rising above the substrate, each dielectric region having a sidewall abutting at least one of the first areas, wherein at least a top portion of the sidewall is exposed;

a first conductive layer over the one or more first areas, the first conductive layer being insulated from the one or more first areas, the first conductive layer providing a first portion of a conductive floating gate for each nonvolatile memory cell;

(2) removing material from at least the top exposed portion of each sidewall of each said dielectric region, to recess the top portion of the sidewall laterally away from the adjacent first portion of the floating gate;

(3) forming a second conductive layer over the one or more first areas, the second conductive layer contacting the first conductive layer and providing a second portion of the floating gate for each nonvolatile memory cell, the second conductive layer abutting the top recessed sidewall portions of said dielectric regions.

2. The method of Claim 1 further comprising:

forming a dielectric layer over the first and second conductive layers;

forming a third conductive layer on the dielectric layer, to provide a control gate for each nonvolatile memory cell.

3. The method of Claim 1 wherein the dielectric region has a portion overlapping at least one of the first areas, but a top portion of the dielectric region does not overlap the first areas.

4. The method of Claim 3 wherein the top portion of the dielectric region is laterally offset from the first areas.

5. The method of Claim 3 further comprising:

forming a dielectric layer over the first and second conductive layers;

forming a third conductive layer on the dielectric layer, to provide a control gate for each nonvolatile memory cell;

etching the third conductive layer and the first conductive layer to pattern the floating gates and the control gates.

6. The method of Claim 1 wherein the first conductive layer is formed after the dielectric regions.

7. The method of Claim 1 wherein the first conductive layer is before the dielectric regions.

8. The method of Claim 1 wherein the operation (1) comprises forming one or more trenches in the semiconductor substrate, wherein in said dielectric regions, said portions below the top surface of the substrate are located in the one or more trenches.

9. The method of Claim 8 further comprising etching the substrate to form the trench for each dielectric region.

10. The method of Claim 1 wherein the operation (2) comprises isotropic etching of the dielectric regions.

11. The method of Claim 1 wherein in said structure obtained in the operation (1), the top surfaces of the dielectric regions are higher than the top surface of the first layer.

12. The method of Claim 1 wherein at a conclusion of the operation (2), the top surfaces of the dielectric regions are higher than the top surface of the first layer.

13. The method of Claim 1 wherein at each floating gate, the top portion of the second layer is not higher than the top portion of each dielectric region adjacent to the floating gate.